L Number	Hits	Search Text	DB	Time stamp
6	5	"6092116"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/20 11:07
10	2	6304578.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/20 14:05
-	6	("5583861" or "6034959" or "5610914").pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/18 16:04
-	2	(("5583861" or "6034959" or "5610914").pn.) and priorit$	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/18 17:25
-	1815	(exceed$ near5(level or threshold))with(priorit$ or overrun or overflow or(over adj(run$4 or flow$3)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/18 20:44
-	230	((exceed$ near5(level or threshold))with(priorit$ or overrun or overflow or(over adj(run$4 or flow$3)))) with(buffer or channel)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/18 17:49
-	182	(((exceed$ near5(level or threshold))with(priorit$ or overrun or overflow or(over adj(run$4 or flow$3)))) with(buffer or channel)) and(@ad<20000719 or @prad<20000719 or @rlad<20000719)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/20 14:05
-	11912	(((exceed$)near5(level or threshold))or full)near4 buffer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/18 20:56
-	48	((chang$3 or increas$3 or higher)near5 priority)with ((((exceed$)near5(level or threshold))or full)near4 buffer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/18 20:48
-	15096	channel near5 buffer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/18 20:57
-	31	(channel near5 buffer) and (((((exceed$)near5(level or threshold))or full)near4 buffer) with priorit$)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/18 20:57
-	248	((((exceed$)near5(level or threshold))or full)near4 buffer) with priorit$	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/18 21:04

US005970069A

United States Patent [19]

Kumar et al.

[11] **Patent Number: 5,970,069**

[45] **Date of Patent: Oct. 19, 1999**

[54] **SINGLE CHIP REMOTE ACCESS PROCESSOR**

[75] Inventors: **Shailendra Kumar**, San Jose, Calif.; **Christopher D. Sonnek**, North St. Paul, Minn.

[73] Assignee: **LSI Logic Corporation**, Milpitas, Calif.

[21] Appl. No.: 08/840,875

[22] Filed: Apr. 21, 1997

[51] Int. Cl.[6] H04L 12/28; H04J 3/16

[52] U.S. Cl. 370/402; 370/401; 370/466

[58] Field of Search 370/351, 355, 370/357, 353, 389, 401, 402, 465, 466, 463, 467

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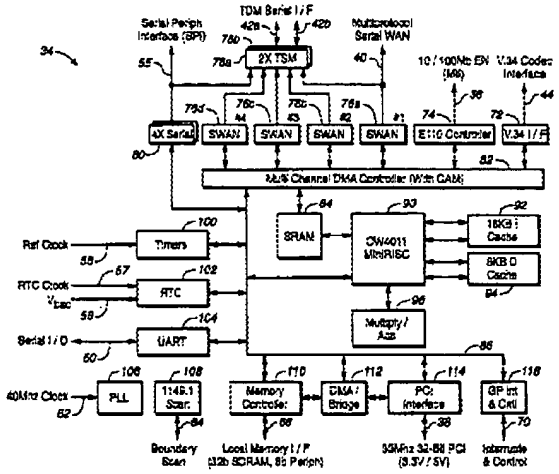
Attorney, Agent, or Firm—Wiseman, Champlin & Kelly, P.A.

[57] **ABSTRACT**

A single chip integrated remote access processor circuit has a plurality of communication interface units, including a local area network (LAN) interface unit, a first multi-protocol serial wide area network (SWAN) interface unit, a telephony codec-decoder interface unit and a peripheral component interface (PCI) unit. A data routing control circuit is coupled to the plurality of communication interface units for controlling data transfer between the interface units.

18 Claims, 83 Drawing Sheets



US-PAT-NO: 5970069

DOCUMENT-IDENTIFIER: US 5970069 A

TITLE: Single chip remote access processor

--------- KWIC --------

Application Filing Date - AD (1):
19970421

Detailed Description Text - DETX (236):
DMAC arbitration for the RAP internal bus 86 alternates between input and output. Arbitration for channel service uses a two priority method based on communication channel FIFO status. Each serial port has programmable thresholds. Those channels with data levels exceeding threshold on receive, or below threshold during transfer are given higher priority than other channels. This allows the DMAC 82 to adapt to peaks in data transfer rate and allows high speed and low speed channels to peacefully coexist.